AMD SB600 Register Programming Requirements (Public Version)

Technical Reference Manual
Rev. 3.02

P/N: 46156_sb600_rpr_pub_3.02

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DISCLAIMER

The information contained in this manual has been carefully checked and is believed to be entirely reliable. No responsibility is assumed for inaccuracies. AMD reserves the right to make changes at any time to improve design and supply the best product possible.

Table of Contents

1 Introduction

1.1 About This Manual

This document lists the register settings required for the proper operation of the AMD SB600. The document will be updated periodically with new or revised settings. Please refer to the latest updated document.

Warning: Customers should use these register settings without any modifications. They are based on numerous qualification and verification procedures, and AMD is not responsible for any abnormal operations of the system that may occur due to modifications of these recommended settings.

This document should be used in conjunction with the *AMD SB600 BIOS Developer's Guide*.

Note: In this document, changes/additions from the previous release are highlighted in red. Refer to the *Appendix: Revision History* at the end of this document for a detailed revision history.

1.2 Features of the AMD SB600

CPU Interface

- Supports both Single and Dual core AMD CPUs
  - Desktop: Athlon 64, Athlon 64 FX, Athlon 64 X2, Sempron, Opteron, dual-core Opteron
  - Mobile: Athlon XP-M, Mobile Athlon 64, Turion 64, Mobile Sempron

PCI Host Bus Controller

- Supports PCI Rev. 2.3 specification
- Supports PCI bus at 33MHz
- Supports up to 6 bus master devices
- Supports 40-bit addressing
- Supports interrupt steering for plug-n-play devices
- Supports concurrent PCI operations
- Supports hiding of PCI devices by BIOS/hardware
- Supports spread spectrum on PCI clocks

USB controllers

- 5 OHCI and 1 EHCI Host controllers to support 10 USB ports
- All 10 ports are USB 1.1 ("Low Speed", "Full Speed") and 2.0 ("High Speed") compatible
- Supports ACPI S1~S5
- Supports legacy keyboard/mouse
- Supports USB debug port
- Supports port disable with individual control

SMBus Controller

- SMBus Rev. 2.0 compliant
- Support SMBALERT # signal / GPIO

Interrupt Controller

- Supports IOAPIC/X-IO APIC mode for 24 channels of interrupts
- Supports 8259 legacy mode for 15 interrupts
- Supports programmable level/edge triggering on each channels
- Supports serial interrupt on quiet and continuous modes

DMA Controller

- Two cascaded 8237 DMA controllers

- Supports PC/PCI DMA
- Supports LPC DMA
- Supports type F DMA

LPC host bus controller

- Supports LPC based super I/O and flash devices
- Supports two master/DMA devices
- Supports TPM version 1.1/1.2 devices for enhanced security
- Supports SPI devices

SATA II AHCI Controller

- Supports four SATA ports, complying with the SATA 2.0 specification
- Supports SATA II 3.0GHz PHY, with backward compatibility with 1.5GHz
- Supports RAID striping (RAID 0) across all 4 ports
- Supports RAID mirroring (RAID 1) across all 4 ports
- Supports RAID 10 (4 ports needed)
- Supports both AHCI mode and IDE mode
- Supports advanced power management with ACHI mode

IDE Controller

- Single PATA channel support
- Supports PIO, Multi-word DMA, and Ultra DMA 33/66/100/133 modes
- 32x32byte buffers on each channel for buffering
- Swap bay support by tri-state IDE signals
- Supports Message Signaled Interrupt (MSI)
- Integrated IDE series resistors

AC Link interface

- Supports for both audio and modem codecs
- Compliant with AC-97 codec Rev. 2.3
- 6/8 channel support on audio codec
- Multiple functions for audio and modem Codec operations
- Bus master logic
- Supports up to 3 codecs simultaneously
- Supports SPDIF output
- Separate bus from the HD audio

HD Audio

- 4 Independent output streams (DMA)
- 4 Independent input streams (DMA)
- Up to 16 channels of audio output per stream
- Supports up to 4 codecs
- Up to 192kHz sample rate
- Up to 32-bit per sample
- Message Signaled Interrupt (MSI) capability
- 64-bit addressing capability for MSI
- 64-bit addressing capability for DMA bus master
- Unified Audio Architecture (UAA) compatible
- HD Audio registers can be located anywhere in the 64-bit address space

Timers

- 8254-compatible timer
- Microsoft High Precision Event Timer (HPET)
- ACPI power management timer

RTC (Real Time Clock)

- 256-byte battery-backed CMOS RAM
- Hardware supported century rollover
- RTC battery monitoring feature

Power Management

- ACPI specification 2.0 compliant power management schemes

    - Supports C2, C3, C4, ACPI states
    - Supports C1e and C3 pop-up
    - Supports S0, S1, S2, S3, S4, and S5
- Wakeup events for S1, S2, S3, S4/S5 generated by:
    - Any GEVENT pin
    - Any GPM pin
    - USB
    - Power button
    - Internal RTC wakeup
    - SMI# event
- Full support for On-Now™
- Supports CPU SMM, generating SMI# signal upon power management events
- GPIO supports on external wake up events
- Supports CLKRUN# on PCI power management
- Provides clock generator and CPU STPCLK# control
- Support for ASF

Hardware Monitor

- Supports 3 Independent FAN Control outputs
- Supports 1 AMDSI function

Note: SB600 does not support thermal diode temperature sensing function.

1.3 AMD SB600 Block Diagrams

This section contains two block diagrams for the SB600. *Figure 1* below shows the SB600 internal PCI devices with their assigned bus, device, and function numbers. *Figure 2* below shows the SB600 internal PCI devices and the major function blocks.

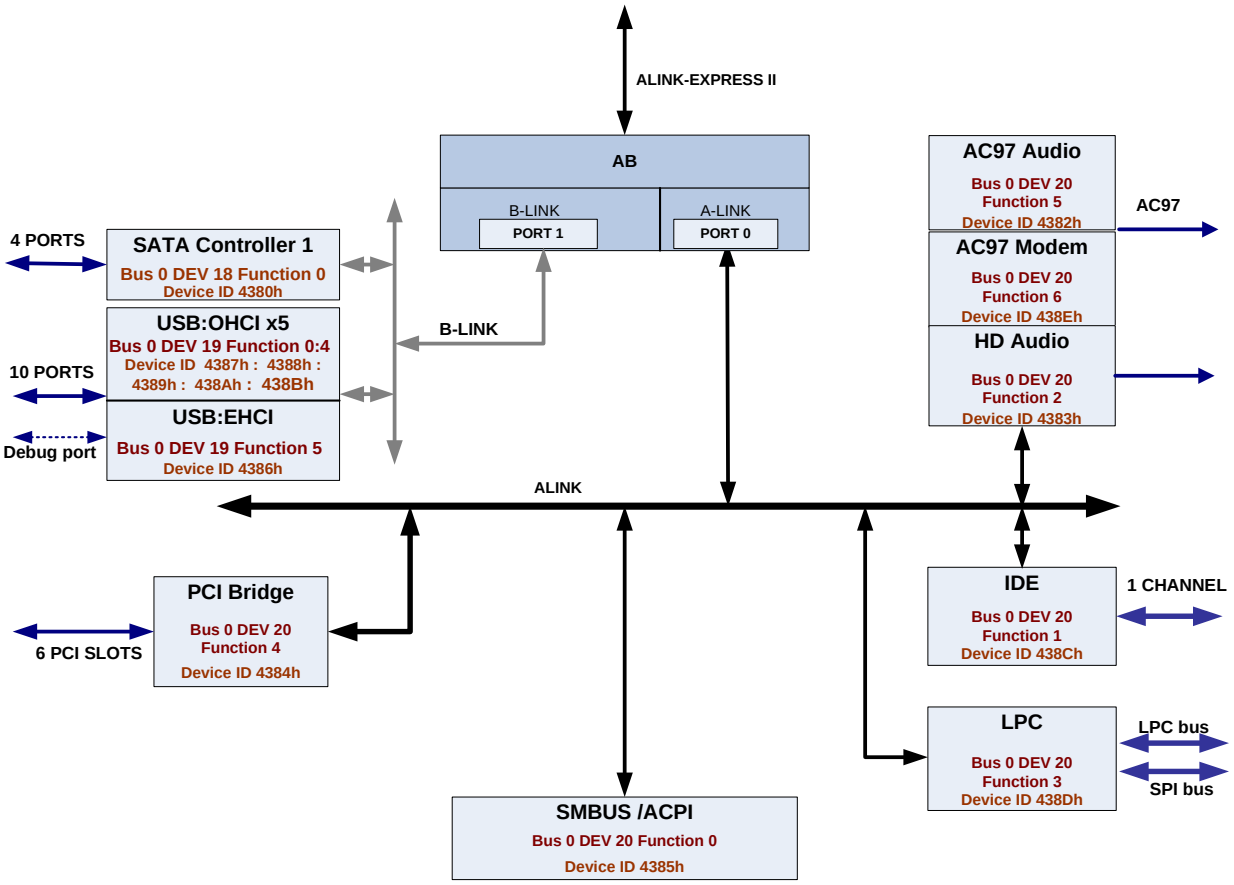

Figure 1 AMD SB600 PCI Internal Devices

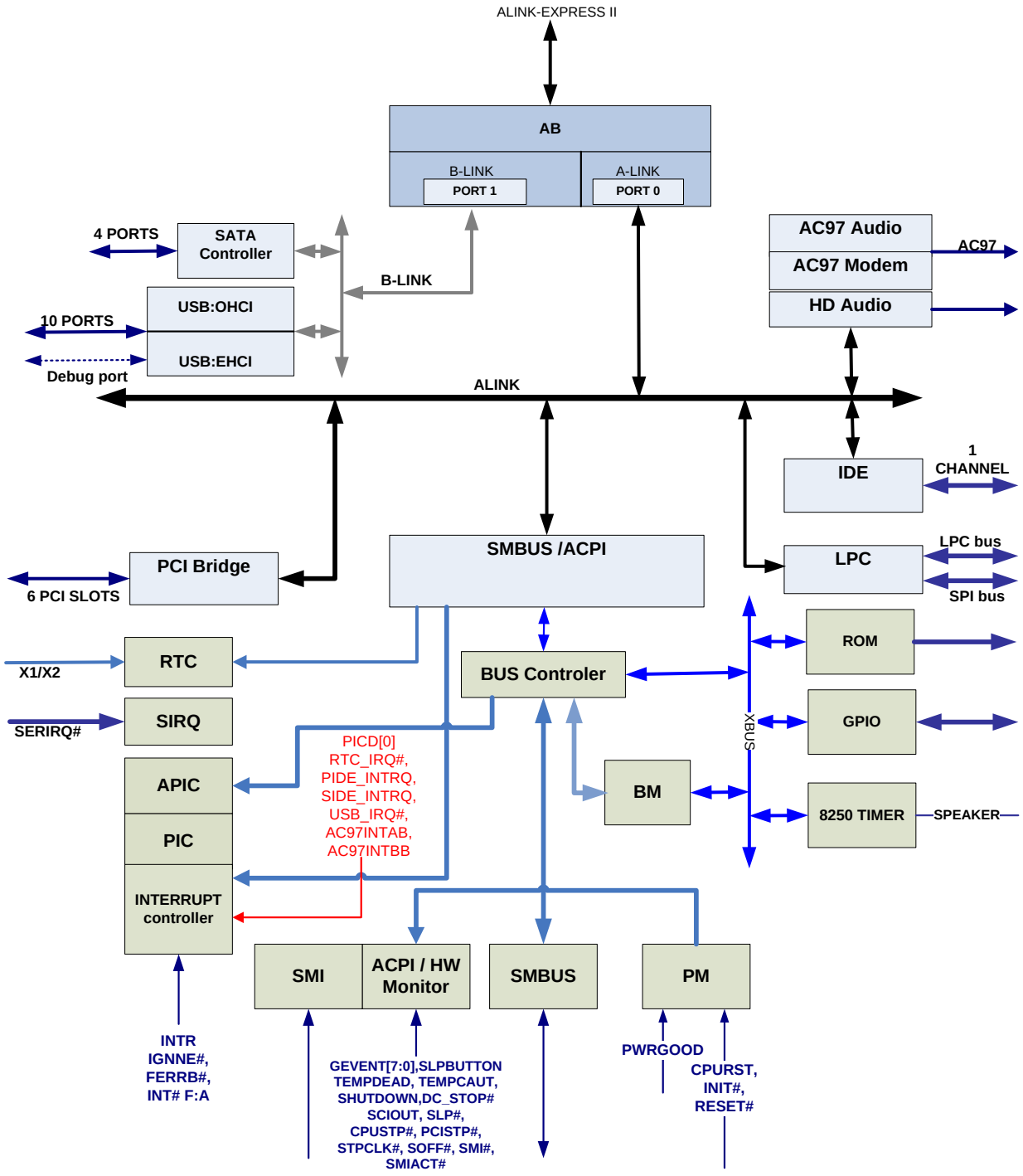

Figure 2 AMD SB600 PCI Internal Devices and Major Function Blocks

1.4 Register Reference Information

Tables within this document contain information showing the applicable revision, recommended settings, and comments associated with the register. Consider the following example:

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x52[5:0] = 08h	Recommended Delay for S3/S4/S5 resume sequence

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx.
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

- ASIC Rev → All Revs SB600 = Applicable to all revisions of the SB600
- Register Settings → Recommended register setting with the register name.

For more detailed information about the registers found within this document refer to the *AMD SB600 Register Reference Guide (RRG -xxxSB600-xx)* document. The applicable sections in the register reference guide where the information can be found are marked with “x” in the tables in this document.

2 ACPI/SMBUS Controller (bus-0, dev-20, fun-0)

2.1 Identifying Chip Revision ID

ASIC Rev	Register Settings
SB600 A11	Smbus_PCI_config 0x08 [7:0] = 11
SB600 A12	Smbus_PCI_config 0x08 [7:0] = 12
SB600 A13	Smbus_PCI_config 0x08 [7:0] = 13
SB600 A21 and above	SMbus_PCI_config 0x08h = 13 if Smbus_PCI_Config 0x70[8] = 0 SMbus_PCI_config 0x08h = 14 if Smbus_PCI_Config 0x70[8] = 1

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		x						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.2 Identifying the K8 Platform

ASIC Rev	Register Settings
All Revs SB600	Check Smbus_PCI_config 0x34: 0x00 = P4 (Intel) 0xB0 = K8 (AMD)

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		x						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.3 K8 Platform Related Settings

2.3.1 Enabling K8 INTR

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0x62 [2] = 1	This bit enables K8 INTR. This bit must be set to 1 for the K8 (AMD) platform.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		x						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.3.2 WakeIO Base Address

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0xF4 [15:0]	For K8 (AMD) platforms only. This register is the I/O base address used to generate the C-state wake event by the processor. The BIOS should program this register with the I/O base address for the SB600. The base address in the CPU should also be programmed. The CPU (K8) can use it to generate an I/O write to the SB to wake the system from the C-state.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		x						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.3.3 C-State and VID/FID Change for the K8 Platform

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	BIOS should not report real ARB_DIS to OS if C3 pop-up is enabled.	With C3 pop-up, ARB_DIS should not be set or cleared by software.
All Revs SB600	PM_IO 0x9A [5] = 1	For system with dual core CPU, set this bit to 1 to automatically clear BM_STS when the C3 state is being initiated.
All Revs SB600	PM_IO 0x9A [4] = 1	For system with dual core CPU, set this bit to 1 and BM_STS will cause C3 to wakeup regardless of BM_RLD.
All Revs SB600	PM_IO 0x9A [2] = 1	Enables pop-up for C3 For internal bus mastering or BmReq# from the NB, the SB will de-assert LDTSTP# (pop-up) to allow DMA traffic, then assert LDTSTP# again after some idle time.
All Revs SB600	PM_IO 0x8F [5] = 1	Ignore BM_STS_SET message from NB
All Revs SB600 + RS4x0 ASIC family of NB	PM_IO 0x8F [4] = 1	The SB will monitor BmReq# when C3 pop-up. The SB will pop-up to C2 when the BmReq# is active.
All Revs SB600 + RS690 ASIC family of NB	PM_IO 0x8F [4] = 0	The SB will not monitor BmReq# when C3 pop-up. The SB will pop-up to C2 when AllowLdtStop is active. BmReq# activity is combined on AllowLdtStop in the RS690 ASIC family of NB. This setting is mandatory to allow for the proper operation of C3 pop-up for systems that use the RS690 NB with the SB600.
All Revs SB600	PM_IO 0x8B = 0x01	StutterTime = 01h for minimum LDTSTP# assertion duration of 1us in C3.
All Revs SB600	PM_IO 0x8A = 0x90	Bit[7] = Enable StutterMode for C3 Bits[6:4] = VidFidTime = 001b for LDTSTP# assertion duration of 2us in VID/FID change.
SB600 A21 and above	PM_IO 0x89 = 0x10	This provides 16us delay before the assertion of LDTSTP# when C3 is entered. The delay will allow USB DMA to go on in a continuous manner.

ASIC Rev	Register Settings	Function/Comment
SB600 A11 to A13	PM_IO 0x88 = 0x06	LdtStartTime = 06h for minimum LDTSTP# de-assertion duration of 6us in StutterMode. This is to guarantee that the HT link has been safely reconnected before it can be disconnected again. If C3 pop-up is enabled, the 6us also serves as the minimum idle time before LDTSTP# can be asserted again. This allows DMA to finish before the HT link is disconnected.
SB600 A21 and above	PM_IO 0x88 = 0x10	The longer delay of 16us will allow USB DMA to go on in a continuous manner.
All Revs SB600	PM_IO 0x7C [0] = 1	Set this bit to 1 to allow wakeup from C3 if break event happens before LDTSTOP# assertion.
All Revs SB600	PM_IO 0x68 [1] = 0 PM_IO 0x8D [6] = 0	These two bits are for the P4 platform only. They must be 0 for the K8 platform.
All Revs SB600	PM_IO 0x61 [2] = 0	If this bit is set to 1, the BmReq# input or internal bus mastering will cause a C3 break event. This bit should be 0 if C3 pop-up is enabled.
SB600 A21 and above	PM_IO 0x52 [7] = 1	Set this bit to 1 to allow pop-up request being latched during the minimum LDTSTP# assertion time. Pop-up will happen thereafter even if the request has gone.
All Revs SB600	PM_IO 0x42 [2] = 0	If this bit is set to 1, the SB will convert C2 into C3, i.e. LVL2 read is treated the same as LVL3 read by hardware. This feature needs to be turned off because of the following reason. Some USB applications require continuous DMA transfer and are very sensitive to C3. The SB is configured to allow USB to set BM_STS and cause immediate exit from C3. When BM_STS is set the OS will issue C2 instead of C3. If C2 is converted into C3, the exit will not happen until the next interrupt because the OS does not set BM_RLD before issuing C2 and BM_STS is not considered a break event. Setting PM_IO 0x9A [4] = 1 can guarantee immediate exit in this case. But then the C2 to C3 conversion does not offer any power saving benefit. The feature is pending for future exploration.

Note: C3 pop-up is recommended for all systems.

Quick reference: Settings for dual-core system:
PM_IO 0x9A [5] = 1
PM_IO 0x9A [4] = 1
PM_IO 0x9A [2] = 1
PM_IO 0x8F [5] = 1
PM_IO 0x8F [4] = (1 for SB600 + RS4x0 NB; 0 for SB600 + RS690 NB)
PM_IO 0x8B = 0x01
PM_IO 0x8A = 0x90
PM_IO 0x88 = 0x06 (Rev A13 = 06h / Rev A21 = 10h)
PM_IO 0x7C [0] = 1
PM_IO 0x68 [1] = 0
PM_IO 0x8D [6] = 0
PM_IO 0x61 [2] = 0
PM_IO 0x42 [2] = 0

Quick reference: Settings for single-core system:

PM_IO 0x9A [5] = 0
PM_IO 0x9A [4] = 0
PM_IO 0x9A [2] = 1
PM_IO 0x8F [5] = 1

ASIC Rev	Register Settings	Function/Comment
	PM_IO 0x8F [4] = (1 for SB600 + RS4x0 NB; 0 for SB600 + RS690 NB) PM_IO 0x8B = 0x01 PM_IO 0x8A = 0x90 PM_IO 0x88 = 0x06 (Rev A13 = 06h / Rev A21 = 10h) PM_IO 0x7C [0] = 1 PM_IO 0x68 [1] = 0 PM_IO 0x8D [6] = 0 PM_IO 0x61 [2] = 0 PM_IO 0x42 [2] = 0	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.3.4 S3/S4/S5 Function for the K8 Platform

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x52[5:0] = 0x08	Recommended delay setting for S3/S4/S5 resume sequence. Note: Bit [7] of PMIO register 52h is now used for the debug feature on ASIC revision A21. This bit should not be modified when programming the resume delay. The resume delay is controlled by bits [5:0] only. On ASIC revision A13 bits [7:6] are not used.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.3.5 Enabling Non-Posted Memory Write for the K8 Platform

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	AXINDC:0x10 [9] = 1	Enables non-posted memory write.

Programming Sequence:

```
OUT AB_INDX, 0x00000030    // Load AB_INDX with pointer to AX_INDXC
OUT AB_DATA, 0x00000010    // Write 0x10 to AX_INDXC
OUT AB_INDX, 0x00000034    // Load AB_INDX with pointer to AX_DATAC
IN  AB_DATA, TMP           // Read PCIE_CTL register (AXINDC:0x10)
OR TMP,      0x00000200    // Set bit 9
OUT AB_DATA, TMP           // Set PCIE_HT_NP_MEM_WRITE.
```

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

2.4 ThermTrip Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x68 [3]	0 = Disable the ThermTrip function on GEvent#2 pin. 1 = Enable the ThermTrip function on GEvent#2 pin.
	PM_IO 0x55 [0] = 1	With this bit set to 1, the ThermTrip function once activated will shutdown the system.
	PM_IO 0x67 [6:5]	These two bits are used to set the polarity of the ThermTrip and the TempCaut signals. Default = 00 (this means that the signals are active low).

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.5 Sx State Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x65 [7] = 0	Use 8us clock for delays in the S-state resume timing sequence.
	PM_IO 0x68 [2] = 1	Delay the APIC interrupt to the CPU until the system has fully resumed from the S-state.

Note: These 2 registers need to be set correctly for the S-state to work properly. Otherwise the system may hang during resume from the S-state.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.6 Output Drive Strength Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0xC0 [29:0]	These register bits configure the drive strength of each individual bus. Refer to the *AMD SB600 Register Reference Manual*, SMBUS section describing the PCI config C0h for the recommended driving strength values.

Note: For more detail please refer to the *AMD SB600 Register Reference Manual*.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.7 SUS_STAT# Enhancement

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x7C[5]	1 = Enable SUS_STAT# enhancement. 0 = Disable SUS_STAT# enhancement. If enabled SUS_STAT# assertion will be extended until after the SB has fully resumed from the S3/4/5 state.

Note: This is a precautionary measure to suppress a glitch on the CKE pin for some early NB revisions on the P4 platform. Enable it only if the NB requires.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.8 Enabling IRQ1/12 Filtering

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0x62 [1:0] = 0h	The filtering for IRQ1 and IRQ12 should be disabled if previously enabled. The hardware default for these register bits is to disable the IRQ1 and IRQ12 filtering. The BIOS should not program these two bits to 11b after power up.
All Revs SB600	Smbus_PCI_config 0x64 [13] = 1	Delays back to back interrupts to the CPU. The hardware will delay an interrupt for approximately 500ns if there is a pending interrupt. Some applications in PIC mode may not be able to handle back to back interrupts in a short time period. Enabling this bit will prevent the application from encountering back to back interrupts.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.9 IO Trap Settings

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x14 ~ 0x1B, 0xA0 ~ 0xA7	Programmable address ranges for IO trap.
All Revs SB600	PM_IO 0x1C ~ 0x1D, 0xA8 ~ 0xA9	IO trap enable/status registers.
All Revs SB600	**P4 platform:** 1. PM_IO 0x14 ~ 0x1D or 0xA0 ~ 0xA9	ABCFG 0x10090[16] setting is don't-care on the P4 platform.
All Revs SB600	**K8 platform:** 1. ABCFG 0x10090 [16] = 1 2. PM_IO 0x14 ~ 0x1D or 0xA0 ~ 0xA9	ABCFG 0x10090 [16] = 1ensures the SMI# message to be sent before the IO command is completed. The ordering of SMI# and IO is important for the IO trap to work properly on the K8 platform.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
		X	**X**					

2.10 Enabling ACPI Registers

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	1. Assign the IO base address for the following ACPI registers: - AcpiPm1EvtBlk = PM_IO 0x20, 0x21 - AcpiPm1CntBlk = PM_IO 0x22, 0x23 - AcpiPmTmrBlk = PM_IO 0x24, 0x25 - CpuControl = PM_IO 0x26, 0x27 - AcpiGpe0Blk = PM_IO 0x28, 0x29 - AcpiSmiCmd = PM_IO 0x2A, 0x2B - AcpiPmaCntBlk = PM_IO 0x2C, 0x2D - AcpiSsCntBlk = PM_IO 0x2E, 0x2F 2. Set AcpiDecodeEnable - PM_IO 0x0E[3] = 1	The BIOS needs to assign the IO base address for each of the ACPI registers before enabling the ACPI decode. The IO base addresses are defined in PM_IO 0x20 ~ 0x2F registers. Note: The PM_IO 0x20 ~ 0x2F registers are undefined upon the first system power up and may therefore contain random values. If the BIOS enables the ACPI decode without assigning the proper IO base addresses for the ACPI registers, the SB may decode incorrect IO addresses and cause unexpected system behavior.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
		X						

2.11 Legacy DMA Prefetch Enhancement

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0x43 [0] = 0	This bit should be 0 so that the legacy DMA prefetch enhancement is disabled. This ensures the proper operation of the floppy drive.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.12 USB Set BM_STS

ASIC Rev	Register Settings	Function/Comment
All Revs SB600, for P4 system; SB600 A11 to A13 for K8 system	PM_IO 0x66 [6] = 1	Enables the USB controller to force the system out of the C3/4 state when there is DMA initiated by the USB (by setting the BM_STS). This will improve the performance of the latency sensitive USB devices if the C state is enabled.
SB600 A21 and above for K8 system	PM_IO 0x66 [6] = 0	For balanced power saving and USB performance, allow USB DMA to cause pop-up. Other register settings for C state should be followed for the system to work properly.
SB600 A21 and above for P4 system	PM_IO 0x51 [6] = 1	Setting this bit to 1 will hide BM_STS from OS read and will provide improved power saving to the system with USB devices.
Note: Refer to section *5.13* for the corresponding USB register settings that are required to be programmed when the above registers are programmed. For the AMD platform, PM_IO 0x66 [6], and register settings in section *5.13*, should be programmed.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.13 Enabling HPET

ASIC Rev	Register Settings	Function/Comment
SB600 all revisions	Smbus_PCI_config 0x64 [10] = 1	Enables the HPET interrupt.
SB600 A13 and above	PM_IO 0x9A [7] = 1 PM_IO 0x9F [5] = 1 PM_IO 0x9E [7] = 1 PM_IO 0x9E [6] = 1	Enables HPET periodical mode.
SB600 A21 and above	PM_IO 0x55 [7] = 1	Hides SM bus controller Bar1 where stores HPET MMIO base address.
SB600 A21 and above	PM_IO 0x52 [6] = 1	Make HPET MMIO decoding controlled by the memory enable bit in command register of LPC ISA bridge.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.14 ASF Remote Control Action

ASIC Rev	Register Settings	Function/Comment
SB600 A13 and above	PM_IO 0x9F [6] = 1	Setting this bit to 1 will prevent the ASF master from interfering with the ASF slave operation.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.15 C-State Reset

ASIC Rev	Register Settings	Function/Comment
SB600 A13 and above	PM_IO 0x9F [7] = 1	Setting this bit to 1 will reset the state machine of C state when PCIRST# is asserted.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.16 PCI Clock Period

ASIC Rev	Register Settings	Function/Comment
SB600 A13 and above	PM_IO 0x53 [7] = 1	By setting this bit to 1, PCI clock period will increase to 30.8 ns.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.17 Disabling SMBUS MSI Capability

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0xAD [7] = 0	Disables MSI capability.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.18 Enabling Spread Spectrum

ASIC Rev	Register Settings	Function/Comment
SB600 A13 and above	PM_IO 0x42 [7] = 1	Enables Spread Spectrum on PCI clocks with -1.5% spread.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.19 Disabling Timer IRQ Enhancement

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0xAE [5] = 1	Disables Timer IRQ enhancement for the proper operation of the 8254 timer.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.20 Toggle CPU_PG On Any Reset

ASIC Rev	Register Settings	Function/Comment
SB600 A13 and above	PM_IO 0x42 [3] = 0	If the BIOS has previously programmed the register x42[3] to 1 it should be changed to not program this register bit. The default power up value is 0 so it should be left at this value. Note: This bit enables or disables the SB capability to toggle the CPU Power Good signal during system reset. For some INTEL CPUs there are timing references in the spec which refer to CPU PG. So, for these CPUs, enabling this feature will allow the timing to be measured with respect to CPU Power Good. There is no functional impact with this feature when either enabled or disabled. With the feature enabled, system hang issues are encountered with Conroe ® CPU. The hang is caused because the CPU is clearing the internal registers on CPU Power Good transition. Therefore, this feature should be turned OFF for all CPUs to avoid possible system hang issues.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.21 PLL Reset

ASIC Rev	Register Settings	Function/Comment
SB600 A21 and above	PM_IO 0x86 [7] = 1	Resets PLL whenever the system gets reset.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.22 PCIE Native Mode

ASIC Rev	Register Settings	Function/Comment
SB600 A21 and above	PM_IO 0x55 [3] = 1	Enables PCIE native mode.
SB600 A21 and above	PM_IO 0x55 [4] = 1	Disables PCIE_WAK_DIS/PCIE_WAK_STS function
SB600 A21 and above	PM_IO 0x55 [5] = 1	Forces the non-generation of SCI when seeing PCIE wake event.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

2.23 Disabling Legacy USB Fast SMI#

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0x62 [5] = 1	For the K8 system, legacy USB can request SMI# to be sent out early before IO completion. Some applications may have problems with this feature. The BIOS should set this bit to 1 to disable the feature. This bit has no effect on the P4 system.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		x						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

2.24 ASF Programming Sequence

- Step 1:Set the base address of ASF Io space by programming bits [15:4] of Sm cfg space reg 58h:

ASFSMbusIoBase- RW - 16 bits - [PCI_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
ASFSMBusEnable	0	0h	0 – Disable ASF controller 1 – Enable ASF controller
Reserved	3:1	000b	
ASFSMBase	15:4	FFFh	ASF SM bus controller Io base address

- Step 2: Enable the ASF controller by programming bit [0] of Sm cfg space reg 58h:

ASFSMbusIoBase- RW - 16 bits - [PCI_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
ASFSMBusEnable	0	0h	0: Disable ASF controller 1: Enable ASF controller
Reserved	3:1	000b	
ASFSMBase	15:4	FFFh	ASF SM bus controller Io base address

- Step 3: Set the ASF Sensor/Legacy sensor base address by programming ASF Io space reg 0Fh:

SensorAdr– RW - 8 bits - [ASF_IO: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
SensorAdr	7:1	00h	SM address of Sensor.

- Step 4: Enable Legacy Sensor support:

SlaveMisc- RW - 8 bits - [ASF_IO: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
SlavePECError	0	0b	RO 0: No PEC error 1: PEC error
SlaveBusCollision	1	0b	RO 0: No BusCollision 1: BusCollision happens
SlaveDevError	2	0b	RO 0: Expected response 1: Unexpected response
WrongSP	3	0b	RO 0: No SP error 1: No SP when turn to read
Reserved	4	0b	
SuspendSlave	5	0b	RW Write 1 to Suspend (stop) ASF Slave state machine
KillSlave	6	0b	RW Write 1 to reset Slave ASF Slave state machine

SlaveMisc- RW - 8 bits - [ASF_IO: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
LegacySensorEn	7	0b	RW 0: Disable Legacy Sensor 1: Enable Legacy Sensor

- Step 5: Select the Alert status to be returned by the Legacy sensor:

  Legacy sensor0:
  Address is SensorAdr
  Polling command is 23h
  Returned status mapping by Legacy sensor polling command:
  Bit [0]: Temp0
  Bit [1]: Temp1
  Bit [2]: Temp2
  Bit [3]: Temp3
  Bit [4]: AMDSI
  Bit [5]: FanSpeed0
  Bit [6]: FanSpeed1
  Bit [7]: FanSpeed2

  Legacy sensor1:
  Address is SensorAdr+1
  Legacy sensor1 polling command is 23h
  Returned status mapping by Legacy sensor polling command:
  Bit [0]: AnalogIo0(VIN0)
  Bit [1]: AnalogIo1(VIN1)
  Bit [2]: AnalogIo2(VIN2)
  Bit [3]: AnalogIo3(VIN3)
  Bit [4]: AnalogIo4(VIN4)
  Bit [5]: AnalogIo5(VIN5)
  Bit [6]: AnalogIo6(VIN6)
  Bit [7]: AnalogIo7(VIN7)

  Select status.

StatusMask0– RW - 8 bits - [ASF_IO: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Temp0StatusEnable	0	0b	1: Report Temp0 status to ASF 0: No report
Temp1StatusEnable	1	0b	1: Report Temp1 status to ASF 0: No report
Temp2StatusEnable	2	0b	1: Report Temp2 status to ASF 0: No report
Temp3StatusEnable	3	0b	1: Report Temp3 status to ASF 0: No report
AMDSIStatusEnable	4	0b	1: Report AMDSI status to ASF 0: No report
FanSpeed0StatusEnable	5	0b	1: Report Fan0 Speed Status to ASF 0: No report
FanSpeed1StatusEnable	6	0b	1: Report Fan1 Speed Status to ASF 0: No report
FanSpeed2StatusEnable	7	0b	1: Report Fan2 Speed Status to ASF 0: No report

StatusMask1– RW - 8 bits - [ASF_IO: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
AnalogIo0StatusEnable	0	0b	1: Report AnalogIo0 status to ASF 0: No report
AnalogIo1StatusEnable	1	0b	1: Report AnalogIo1 status to ASF 0: No report
AnalogIo2StatusEnable	2	0b	1: Report AnalogIo2 status to ASF 0: No report
AnalogIo3StatusEnable	3	0b	1: Report AnalogIo3 status to ASF 0: No report
AnalogIo4StatusEnable	4	0b	1: Report AnalogIo4 status to ASF 0: No report
AnalogIo5StatusEnable	5	0b	1: Report AnalogIo5 status to ASF 0: No report
AnalogIo6StatusEnable	6	0b	1: Report AnalogIo6 status to ASF 0: No report
AnalogIo7StatusEnable	7	0b	1: Report AnalogIo7 status to ASF 0: No report

- Step 6: Enable PEC if ASD supported PEC:

HostControl – RW - 8 bits - [ASF_IO: 02h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
KillHost	1	0b	0: Enable SM master 1: Reset SM master
Protocol	4:2	000b	000: Quick 001: Byte 010: Byte Data 011: Word Data 100: Process call 101: Block
PECAppend	5	0b	0: No PEC append 1: Automatic PEC append. ASF HC calculates CRC code and append to the tail of the data packets.
Start	6	0b	WO: 0: Always read 0 on reads 1: Writing 1 to initiate the command
PECEnable	7	0b	0: PEC disable 1: PEC enable, enable CRC checking when ASF HC presents as SM master and SM slave.

- Step 7: Set Remote Control Address

RemoteCtrlAdr– RW - 8 bits - [ASF_IO: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
RemoteCtrlAdr	7:1	00h	SM address of Remote Control device.

	Control command	Control data value
Reset	00h	00h
PowerUp	01h	00h
PowerDown	02h	00h
PowerCycle	03h	00h

- Step 8: ASF table

  Ensure that the Legacy sensor address in the ASF table reports the same value as the one in the ASF Legacy sensor address register.

  Ensure that the Remote control address in the ASF table reports the same value as the one in the ASF Remote control address register.

- Step 9: SMBios

  Ensure that the SMBios table is correct

- Step 10: Report the ASF device to the OS in ACPI ASL code.

3 A-Link Express Settings - Indirect I/O Access

Warning: The register settings in this section are for the internal bus interface, and they are listed here for reference only. These settings impact not only the performance of the A-Link Express interface, but also other interfaces. Modifying these registers will impact the overall system stability.

3.1 Defining AB_REG_BAR (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0xF0 [31:0] = AB_REG_BAR	Defines the AB I/O base address. Refer to *AMD SB600 Register Reference Manual, chapter 5: A-Link Express/A-Link Bridge Registers* for more information.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

3.2 Clearing AB_INDX

The programming procedure for the ABCFG registers, as specified in the register reference guide, is to first load AB_INDX with a register's RegSpace and RegAddr; and then access the specified register through AB_DATA. The example below demonstrates how to read ABCFG:10058h:

```
OUT AB_INDX, 0xC0010058    // Set AB_INDX RegSpace=11 RegAddr=0x10058
IN  AB_DATA, TMP
```

For certain revisions of the chip, the ABCFG registers, with an address of 0x100NN (where 'N' is any hexadecimal number), require an extra programming step. This required step is defined in the following table:

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	AB_INDX = 0x00000000	Clears AB_INDX after reading or writing an ABCFG register with an address 0x100NN.

Example Programming Sequence:

```
OUT AB_INDX, 0xC00100NN    // Load AB_INDX with pointer to ABCFG:0x100NN
IN  AB_DATA, TMP           // Read ABCFG 0x100NN
OUT AB_INDX, 0x00000000    // Clear AB_INDX
```

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			
			X					

3.3 Programming the AB registers

The following section lists all the registers that are required to be programmed on power up. These registers are for initializing the AB interface. Section 1.3.1 list the register setting required for Power Management of A-Link.

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	AXCFG: 0x04 [2] = 1	

Programming Sequence:

```
OUT AB_INDX, 0x80000004    // Load AB_INDX with pointer to AXCFG:0x04
IN  AB_DATA, TMP           // Read COMMAND register (AXCFG:0x04)
OR  TMP,     0x00000004    // Set bit 4
OUT AB_DATA, TMP           // Set BUS_MASTER_EN
```

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	
All Revs SB600	IDE prefetch ABCFG 0x10060 [17] = 1 ABCFG 0x10064 [17] = 1 PCIB prefetch ABCFG 0x10060 [20] = 1 ABCFG 0x10064 [20] = 1	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	Function/Comment
SB600 A11 SB600 A12 and above	OHCI prefetch: ABCFG 0x80 [0] = 0 ABCFG 0x80 [0] = 1	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	ABCFG 0x9c [0] = 1	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	ABCFG 0x9c [1] = 1	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	ABCFG 0x80 [17] = 1 ABCFG 0x80 [18] = 1	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	ABCFG 0x94 [20] = 1 ABCFG 0x94 [19:0] = CPU interrupt delivery address [39:20].	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	ABCFG 0x10090 [8] = 1	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	ABCFG 0x54 [23:16] = 0x4 ABCFG 0x10054 [23:16] = 0x4 ABCFG 0x98 [15:12] = 0x4	.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	ABCFG 0x54[24] = 1 ABCFG 0x10054[24] = 1 ABCFG 0x98[11:8] = 0x7	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	ABCFG 0x10054[15:0] =0x07FF	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

3.3.1 Enabling L1 on A-Link Express (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	AXCFG 0x68[1:0] =0x2 AX_INDXP 0xA0[15:12]=0x6	Enables L1 on the A-Link Express. L1 INACTIVITY Timer set to 40 us.

zSATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
			X					

4 PCIB (PCI-bridge, bus-0, dev-20, fun-04)

4.1 Enabling PCI-bridge Subtractive Decode

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x40 [5] = 1 PCIB_PCI_config 0x4B [7]= 1	Enables the PCI-bridge subtractive decode. This setting is strongly recommended since it supports some legacy PCI add-on cards.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.2 PCI-bridge Upstream Dual Address Window

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x50 [0] = 1	PCI-bridge upstream dual address window. This setting is applicable if the system memory is more than 4GB, and the PCI devices can support dual address access.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.3 PCI Bus 64-byte DMA Read Access

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x4B [4] = 1	PCI bus 64-byte DMA read access. Enhances the PCI bus DMA performance.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.4 PCI Bus DMA Write Cacheline Alignment (for All Revisions)

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x40 [1] = 1	Enables the PCIB writes to be cacheline aligned. The size of the writes will be set in the Cacheline Register (PCIB_PCI_config 0x4B[4:0]). Refer to section *4.3* for more information.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.5 Master Latency Timer

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x0D = 0x40 PCIB_PCI_config 0x1B = 0x40	Enables the PCIB to retain ownership of the bus on the Primary side and on the Secondary side when GNT# is de-asserted. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.6 DMA Read Command Match

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x4B[6] = 1	Enables the command matching checking function on "Memory Read" & "Memory Read Line" commands. Some PCI devices may change the "Memory read command" to "Memory read line" command before the data is completed. This bit enables the command matching checking inside the PCIB to work with this kind of device. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.7 Enabling Idle To Gnt# Check

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x4B [0] = 1	When enabled, the PCI arbiter checks for the Bus Idle before asserting GNT#. Note: This setting is recommended.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.8 GNT# Timing Adjustment

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x64 [12] = 1	Adjusts the GNT# de-assertion time. Note: This setting is recommended.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.9 Enabling Fast Back to Back Retry

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x48 [2] = 1	Enables Fast Back to Back transactions support. Note: This setting is recommended

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.10 Enabling Lock Operation

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x48 [3] = 1	This bit should be set to 1 when PCI configuration space PCIB_PCI config 0x40 [2] = 1 for the proper operation of the PCI LOCK# function.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.11 Enabling Additional Optional PCI Clock (PCICLK7)

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x64 [8] = 1	This only applies when PCICLK7/PCIREQ5#/PCIGNT5# are enabled: When this bit is set, PCICLK7, PCIREQ#5, and PCIGNT5# are enabled for PCI use. Since PCICLK7 is not enabled by default (the clock is off), the PCI device which uses this clock may not see the system reset during power-up. To correct this, the BIOS should write to PCIB config 3Eh, bit [6] to assert the additional PCI reset so the device will see a proper reset, as well as to provide the time for its internal PLL to lock. The recommended duration time is at least a few milliseconds. Note: These three pins are enabled as a group, therefore, care should be taken to make sure they are used properly.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.12 Disabling Fewer-Retry Mode

ASIC REV	Register Settings	Function/Comment
SB600 A11~A13	PCIB_PCI_config 0x64 [5:4] = 0x0	Disables the PCIB fewer-retry mode. This applies to SB600 A11~A13 only. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.13 Enabling One-Prefetch-Channel Mode

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x64 [20] = 0x1	Enables One-Prefetch-Channel Mode. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.14 Disabling Downstream Flush

ASIC REV	Register Settings	Function/Comment
SB600 A12	PCIB_PCI_config 0x64 [18] = 0x1	Disables the downstream flush fix. This applies to SB600 A12 only. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.15 Disabling PCIB MSI Capability

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x40 [3] = 0x0	Disables MSI capability.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

4.16 Adjusting CLKRUN#

ASIC REV	Register Settings	Function/Comment
All Revs SB600	PCIB_PCI_config 0x64 [15] = 0x1	If CLKRUN# is enabled, this bit must be set to 1. Note: This setting is mandatory for the proper operation of CLKRUN#. Refer to the AN_SB600AHx document for more details on how to enable CLKRUN# on mobile platforms.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
							X	
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5 USB – OHCI0~4 & EHCI Controller (bus-0, dev-19, fun-00~04 & 05)

Please note the following information for this section:

- EHCI BAR address = EHCI_PCI_config 0x10[31:8]
- EHCI_EOR is the EHCI operation register = EHCI_BAR + 0x20

5.1 Enabling/Disabling OHCI0 ~ 4 and EHCI Controllers (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0x68 [0] = 1 (default)	Enables the EHCI controller.
All Revs SB600	Smbus_PCI_config 0x68 [1] = 1 (default)	Enables the OHCI controller 1 (OHCI0).
All Revs SB600	Smbus_PCI_config 0x68 [2] = 1 (default)	Enables the OHCI controller 2 (OHCI1).
All Revs SB600	Smbus_PCI_config 0x68 [3] = 1 (default)	Enables the OHCI controller 3 (OHCI2).
All Revs SB600	Smbus_PCI_config 0x68 [4] = 1 (default)	Enables the OHCI controller 4 (OHCI3).
All Revs SB600	Smbus_PCI_config 0x68 [5] = 1 (default)	Enables the OHCI controller 5 (OHCI4).

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.2 USB Device Support to Wake Up System From S3/S4 State (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x61 [6] = 1 PM_IO 0x65 [2] = 1 (default)	Enables the USB PME event. Enables USB resume support.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

5.3 USB S4/S5 Wakeup or PHY Power Down Support (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x65 [0] = 0 (default)	This bit = 0 (default) supports USB device wakeup from the S4/S5 state. Set the bit to 1 to disable the USB S4/S5 wakeup function. The analog power supply to USB PHY on the motherboard can be OFF in this case to save S4/S5 power.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

5.4 USB PHY Auto Calibration Setting (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	EHCI_BAR 0xC0 = 0x00020F00	Enables the USB PHY auto calibration resistor to match 45ohm resistance.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.5 USB IN/OUT FIFO Threshold Setting

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	If NB-SB A-link express is 4 lanes: EHCI_BAR 0xA4 = 0x00200040 If NB-SB A-link express is 2 lanes: EHCI_BAR 0xA4 = 0x00200010	Sets IN/OUT FIFO threshold for best performance. The SBIOS needs to detect how many lanes are configured for the NB-SB link to determine the FIFO threshold setting to gain best performance result.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.6 USB Reset Sequence

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x65 [4] = 1 for both the K8 & P4 platforms	Enables the USB controller to get reset by any software that generates a PCIRst# condition. **However, this bit should be cleared before a software generated reset condition occurs during S3 resume** so the USB controller will not lose the connection status during the S3 resume procedure. The software generated PCIRst# conditions include Keyboard Reset, or write to the IO-CF9 register.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

5.7 USB Data Cache Time Out Counter Setting

ASIC Rev	Register Settings	Function/Comment
SB600 A11/A12	EHCI_PCI_Config 0x50 [19:16] = 0xF	Disables the data cache time out counter. When these 4 bits are set to 0xF, the data cache time out counter will never expire.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.8 USB OHCI Dynamic Power Saving Setting

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	OHCI0_PCI_Config 0x50 [16] = 0	Disables the OHCI Dynamic Power Saving feature.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.9 USB EHCI Dynamic Power Saving Setting

Note: This feature is not supported on the SB600 because it does not meet the requirements of AMD internal qualifications and expectations. If this feature is enabled, the power savings produced is negligible.

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	EHCI_BAR 0xBC [12] = 0	Disables the EHCI Dynamic Power Saving feature.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.10 Disabling USB EHCI MSI Capability

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	EHCI_PCI_Config 0x50 [6] = 1	Disables EHCI MSI support.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.11 Disabling USB OHCI MSI Capability

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	OHCI0_PCI_Config 0x40 [12:8] = 0x1F	Disables OHCI MSI support on all 5 OHCI HCs.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.12 Enabling OHCI Prevention of Accessing Invalid Address

ASIC Rev	Register Settings	Function/Comment
SB600 A21 and above	OHCI0_PCI_Config 0x50 [15] = 1	Enables prevention of OHCI accessing the invalid system memory address range.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.13 Disabling C3 Time Enhancement Feature

ASIC Rev	Register Settings	Function/Comment
SB600 A21 and above	EHCI_PCI_Config 0x50 [28] = 0	Disables the C3 time enhancement feature. This is the power up default setting. If the bit was set previously it should be set to 0, or the BIOS should not program it.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.14 Disabling USB PHY PLL Reset Stabilization

ASIC Rev	Register Settings	Function/Comment
SB600 A21 and above	EHCI_PCI_Config 0x54 [0] = 0	Disables USB PHY PLL Reset signal to come from ACPI

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.15 Disabling USB SMI Internal Handshake

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	OHCI0_PCI_Config 0x50 [12] = 1	Disables SMI handshake in between USB and ACPI for USB legacy support. The BIOS should always set this bit to prevent the malfunction on USB legacy keyboard/mouse support.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

5.16 Disabling USB OHCI DMA Cache

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	OHCI0_PCI_Config 0x50 [10] = 0	Disables OHCI 64byte data cache function to avoid potential data packet corruption for USB1.1 device.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
	X							
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6 SATA: (bus 0, dev-18, fun-0)

6.1 Enabling SATA (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0xAC [8] = 1	Enables the SATA controller.
All Revs SB600	Smbus_PCI_config 0xAC [28:26]	SATA interrupt mapping to PCI interrupt pins.
All Revs SB600	SATA_PCI_config 0x40 [0] = 0	This bit needs to be cleared to convert the subclass code register to read-only. Refer to section *6.4* for the SATA subclass programming sequence.
All Revs SB600	SATA_PCI_config 0x46 [7:0]= 10h	Programs watchdog timer with 16 retries before the timer times-out.
All Revs SB600	SATA_PCI_config 0x44 [0] = 1	Enables the SATA watchdog timer register prior to the SATA BIOS post. See Note.
All Revs SB600	SATA_PCI_config 0x40 [2] = 0	For IDE mode hot-plug support. Setting 40[2] could save SATA power when device is not connected. For supporting hot-plug, 40[2] needs to be cleared.
All Revs SB600	SATA_PCI_config 0x40 [5] = 0	This reserved bit should be set to '0' at all times. The hardware power-up default is '0'. The BIOS should not change this setting.
Note: The system may hang during post if this register is not set correctly.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.2 Disabling SATA (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0xAC [8] = 0	Disables the SATA controller. This shuts down most clocks in the SATA controller.
All Revs SB600	Smbus_PCI_config 0xAC [9] = 1	Disables the SATA PHY I2C interface. This setting is mandatory to prevent un-powered SATA from corrupting SMBus controller protocol.
All Revs SB600	Smbus_PCI_config 0xAC [13] = 1 (default)	Enables the power saving mode for the SATA controller. All the SATA Internal clocks will be shutdown when this bit is set and the SATA controller is disabled.
Note: Some board designs may choose to disable the SATA controllers to reduce power consumption.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.3 Disabling Unused SATA Ports (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	SATA_PCI_config 0x40 [16] = 1	When set, SATA port0 is disabled, and port0 clock is shut down.
	SATA_PCI_config 0x40 [17] = 1	When set, SATA port1 is disabled, and port1 clock is shut down.
	SATA_PCI_config 0x40 [18] = 1	When set, SATA port2 is disabled, and port2 clock is shut down.
	SATA_PCI_config 0x40 [19] = 1	When set, SATA port3 is disabled, and port3 clock is shut down.
Note: Some board designs may choose to disable unused SATA ports to reduce power consumption.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.4 SATA Subclass Programming Sequence (for All Revisions)

The SATA controller supports the following modes:

- IDE mode
- AHCI mode
- Raid mode

The SBIOS programs the subclass code and the interface register to enable the SATA controller to be represented as the IDE controller, the AHCI controller, or the Raid controller.

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	1. SATA_PCI_config 0x40 [0] = 1	Enables the subclass code register (PCI config register 0Ah) and the program interface register (PCI config register 09h) to be programmable.
	2. Program SATA Controller mode in a) IDE mode, or SATA_PCI_config 0x09 = 0x8f (default) SATA_PCI_config 0x0A = 0x01 b) AHCI mode, or SATA_PCI_config 0x09 = 0x01 SATA_PCI_config 0x0A = 0x06 c) RAID mode SATA_PCI_config 0x09 = 0x00 SATA_PCI_config 0x0A = 0x04	The SBIOS is required to program the subclass code register of the SATA controller to be represented as the IDE, AHCI, or the RAID controller.
	3. SATA_PCI_config 0x40 [0]= 0	Clears the bit to convert the subclass code register to be a read-only register. The SBIOS is required to complete this step to ensure that the subclass code register be read-only (in order to be PCI compliant).

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.5 SATA PHY Programming Sequence (for All Revisions)

The SBIOS needs to program the SATA controllers in the following sequence. Performing this procedure gives enough time for the SATA controllers to correctly complete SATA drive detection. The SBIOS needs to do the same procedure after the system resumes back from the S3 state.

ASIC Rev	Register Settings	Function/Comment
SB600 A11	1. SATA_PCI_config 0x86 [15:0] = 0x2400	SATA PHY global setting.
SB600 A12 and above	1. SATA_PCI_config 0x86 [15:0] = 0x2C00	
SB600 A11	2. SATA_PCI_config 0x88 [23:0] = 0xB420D8 SATA_PCI_config 0x8C [23:0]= 0xB420D8 SATA_PCI_config 0x90 [23:0] = 0xB420D8 SATA_PCI_config 0x94 [23:0] = 0xB420D8	SATA PHY port setting. See section 6.5.1.
SB600 A12	2. SATA_PCI_config 0x88 [23:0] = 0xB4005A SATA_PCI_config 0x8C [23:0]= 0xB4005A SATA_PCI_config 0x90 [23:0] = 0xB4005A SATA_PCI_config 0x94 [23:0] = 0xB4005A SATA_PCI_config 0xA5 = 0xB8 SATA_PCI_config 0xAD = 0xB8 SATA_PCI_config 0xB5 = 0xB8 SATA_PCI_config 0xBD = 0xB8	
SB600 A13 with SATA PHY AVDD 1.2V (Refer to PA_SB600AHx for more details on the SATA PHY AVDD voltage section)	2. SATA_PCI_config 0x88 [23:0] = 0xB401DA SATA_PCI_config 0x8C [23:0]= 0xB401DA SATA_PCI_config 0x90 [23:0] = 0xB401DA SATA_PCI_config 0x94 [23:0] = 0xB401DA SATA_PCI_config 0xA5 = 0xB8 SATA_PCI_config 0xAD = 0xB8 SATA_PCI_config 0xB5 = 0xB8 SATA_PCI_config 0xBD = 0xB8	
SB600 A13 with SATA PHY AVDD 1.25V	2. SATA_PCI_config 0x88 [23:0] = 0xB401D5 SATA_PCI_config 0x8C [23:0]= 0xB401D5 SATA_PCI_config 0x90 [23:0] = 0xB401D5 SATA_PCI_config 0x94 [23:0] = 0xB401D5 SATA_PCI_config 0xA5 = 0x78 SATA_PCI_config 0xAD = 0x78 SATA_PCI_config 0xB5 = 0x78 SATA_PCI_config 0xBD = 0x78	
SB600 A21	2. SATA_PCI_config 0x88 [23:0] = 0xB401D6 SATA_PCI_config 0x8C [23:0]= 0xB401D6 SATA_PCI_config 0x90 [23:0] = 0xB401D6 SATA_PCI_config 0x94 [23:0] = 0xB401D6 SATA_PCI_config 0xA5 = 0xB8 SATA_PCI_config 0xAD = 0xB8 SATA_PCI_config 0xB5 = 0xB8 SATA_PCI_config 0xBD = 0xB8	

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	~~3. SATA_BAR5 0x12C[31:0] = 0x00000001~~ ~~SATA_BAR5 0x1AC[31:0] = 0x00000001~~ ~~SATA_BAR5 0x22C[31:0] = 0x00000001~~ ~~SATA_BAR5 0x2AC[31:0] = 0x00000001~~	Removes the requirement for software reset. This second reset is redundant since hardware already accomplishes it during power up. Some DVD drives do not function correctly if they encounter a reset sequence soon after completing the first OOB initiated by the hardware reset.
All Revs SB600	~~4. SATA_BAR5 0x12C[31:0] = 0x00000000~~ ~~SATA_BAR5 0x1AC[31:0] = 0x00000000~~ ~~SATA_BAR5 0x22C[31:0] = 0x00000000~~ ~~SATA_BAR5 0x2AC[31:0] = 0x00000000~~	Since we do not need step 3, there is no need for this sequence too.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.5.1 SATA PHY Settings

The SATA PHY settings have been updated in revision 2.3 of this document to increase tolerance to higher jitter levels and therefore to improve the reliability of the drive in these conditions.

6.6 SATA Identification Programming Sequence for IDE Mode (for All Revisions)

6.6.1 SATA Drive Detection (for All Revisions)

The following sequence should be included in the SBIOS drive identification loop for SATA drives detection.

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	1. If any of the SATA port status register SATA_BAR5 + 0x128 [3:0] = 0x3 SATA_BAR5 + 0x1A8 [3:0] = 0x3 SATA_BAR5 + 0x228 [3:0] = 0x3 SATA_BAR5 + 0x2A8 [3:0] = 0x3 Then set SATA_BAR0 + 0x6 = 0xA0 or SATA_BAR0 + 0x6 = 0xB0 or SATA_BAR2 + 0x6 = 0xA0 or SATA_BAR2 + 0x6 = 0xB0 or Go to step (2). Else No drive is attached, exit the detection loop.	SATA_BAR5 + 0x128h : port 0 status register SATA_BAR5 + 0x1A8h : port 1 status register SATA_BAR5 + 0x228h : port 2 status register SATA_BAR5 + 0x2A8h : port 3 status register SATA host and device serial interface communication is done and ready if the SATA port status register = 0x3. for primary master emulation for primary slave emulation for secondary master emulation for secondary slave emulation Otherwise, No SATA drive attached or SATA drive is not ready.

ASIC Rev	Register Settings	Function/Comment
	2. If SATA_BAR0 + 0x6 = 0xA0 and SATA_BAR0 + 0x7 [7] & [3] = 0 Or SATA_BAR0 + 0x6 = 0xB0 and SATA_BAR0 + 0x7[7] & [3] = 0 Or SATA_BAR2 + 0x6 = 0xA0 and SATA_BAR2 + 0x7[7] & [3] = 0 Or SATA_BAR2 + 0x6 = 0xB0 and SATA_BAR2 + 0x7[7] & [3] = 0 then the drive detection is completed Else loop until 30s time out, drive detection fail	SATA_BAR0 + 0x7[7] & [3] = 0 means primary master device ready SATA_BAR0 + 0x7[7] & [3] = 0 means primary slave device ready SATA_BAR2 + 0x7[7] & [3] = 0 means secondary master device ready SATA_BAR2 + 0x7[7] & [3] = 0 means secondary slave device ready There is no SATA device attached on the port if time out occurs (see Note).

Note: Most drives do not need 10s timeout. The 10s timeout is only needed for some particularly large capacity SATA drives, which require a longer spin-up time during a cold boot.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.7 Restoring SATA Registers After S3 Resume State (for All Revisions)

The following registers need to be restored by the SBIOS after S3 resume for the SATA controller.

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	SATA_PCI_config 0x09 [7:0] SATA_PCI_config 0x0A [7:0]	Programmable interface and Subclass code. To program the subclass code register, SATA_PCI_config x40[0] needs to be set. After the subclass is programmed, SATA_PCI_config 0x40[0] needs to be reset.
	SATA_PCI_config 0x44 [0]	Enables the Watch-dog timer for the all ports.
	SATA_PCI_config 0x86 [15:0] SATA_PCI_config 0x88 [23:0] SATA_PCI_config 0x8C [23:0] SATA_PCI_config 0x90 [23:0] SATA_PCI_config 0x94 [23:0]	SATA PHY setting.
	SATA_BAR5 + 0xFC [11] = 0 SATA_BAR5 + 0xFC [27] = 1 Port0: SATA_BAR5 + 0x12C[11:08] = 0x03 Port1: SATA_BAR5 + 0x1AC[11:08] = 0x03 Port2: SATA_BAR5 + 0x22C[11:08] = 0x03 Port3: SATA_BAR5 + 0x2AC[11:08] = 0x03	CAP.SALP, CAP.PSC/CAP.SSC, and PxSCTL.IPM. To hide Support-Aggressive-Link-Power-Management Capability. To program these registers, SATA_PCI_CFG x40[0] needs to be set. After the programming, this bit needs to be reset.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.8 Disabling SATA MSI Capability (for A13 and Above)

For silicon A13 and above, SATA_PCI_config 0x42[7] needs to set to '1' to disable MSI capability.

ASIC Rev	Register Settings	Function/Comment
SB600 A13 and above	SATA_PCI_config 0x42 [7]=1	Disables MSI capability.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.9 Disabling SATA IDP Capability (for A21 and Below)

ASIC Rev	Register Settings	Function/Comment
SB600 A21 and below	SATA_PCI_config 0x40 [25]=1	Disables IDP capability.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.10 Hide Support-Aggressive-Link-Power-Management Capability in AHCI HBA Capabilities Register (For SB600 All Revisions)

The following programming sequence hides the Support-Aggressive-Link-Power-Management capability while SATA is in AHCI mode. As a result, AHCI-aware software will treat PxCMD.ALPE and PxCMD.ASP as reserved. Ultimately, HBA will not auto-generate link requests to Partial/Slumber states since there is no such capability exposed to software. The SBIOS needs to do the same procedure after the system resumes back from the S3 state. This sequence needs to be done before any command issued to SATA controller. Note: Refer to SB600 Errata #15 in ER_IXP600AC13.pdf for more details on this programming sequence.

ASIC Rev	Register Settings	Function/Comment
SB600 All revisions	1. SATA_PCI_config 0x40 [0] = 1	Unlocks the configuration register so that HBA AHCI Capabilities Register can be modified.
	2. SATA_BAR5 + 0xFC [11] = 0 (CFG_CAP_SALP Disabled)	Clearing this bit has the following effects. The Support-Aggressive-Link-Power-Management Capability is hidden from software in AHCI HBA Capabilities Register. As a result, software will not enable the HBA to aggressively enter power-saving (Partial/Slumber) mode.
	3. SATA_PCI_config 0x40 [0]= 0	Clears the bit to lock configuration registers so that AHCI HBA Capabilities Register is read-only.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.11 Disabling SATA Interface Partial/Slumber States Power Management Transitions (For SB600 All Revisions)

The following programming sequence disables SATA interface transitioning to Partial and Slumber states, regardless of the SATA operation mode (IDE, AHCI, or RAID). Effectively, SATA HBA will neither initiate nor accept devices' requests to transition to these two power saving states. The programming sequence is to be done on a per-port basis. The SBIOS needs to do the same procedure after the system resumes back from the S3 state. This sequence needs to be done before any command issued to SATA controller. Note: Refer to SB600 Errata #15 in ER_IXP600AC13.pdf for more details on this programming sequence.

ASIC Rev	Register Settings	Function/Comment
SB600 All revisions	Port0: SATA_BAR5 + 0x12C[11:08] = 0x03 Port1: SATA_BAR5 + 0x1AC[11:08] = 0x03 Port2: SATA_BAR5 + 0x22C[11:08] = 0x03 Port3: SATA_BAR5 + 0x2AC[11:08] = 0x03	Setting PxSCTL (Port X Serial ATA Control) register bits[11:8] (PxSCTL.IPM) to 0x03 will disable interface power management states (both Partial and Slumber). HBA is not allowed to initiate these two states, and HBA must PMNAK any request from devices to enter these states.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.12 Hiding Slumber and Partial State Capabilities in AHCI HBA Capabilities Register (For SB600 All Revisions)

The following programming sequence hides Slumber State Capable and Partial State Capable in HBA Capabilities Registers, while SATA is in AHCI mode. As a result, Slumber/Partial Power State transitions are disabled across all 4 SATA ports, once AHCI-aware software proceeds to disabling all power management related controls. Globally hiding partial and slumber states transition prevents software from manipulating all power management controls and totally disables power management for the whole SATA Host controller. It is the AHCI-aware software's responsibility to proceed to the disabling of all power management related controls for each port, such as PxCMD.ALPE and PxSCTL.IPM.

The SBIOS needs to do the same procedure after the system resumes back from the S3 state. This sequence needs to be performed before any command is issued to the SATA controller.

ASIC Rev	Register Settings	Function/Comment
SB600 All revisions	1. SATA_PCI_config 0x40 [0] = 1	Unlocks the configuration register so that HBA AHCI Capabilities Register can be modified.
	2. SATA_BAR5 + 0xFC [27] = 1 (CFG_CAP_PSC/CFG_CAP_SSC Disabled)	Setting this bit will result in clearing CAP.SSC (Slumber State Capable) and CAP.PSC (Partial State Capable) in AHCI HBA Capabilities Register. Ultimately, software will not be able to manipulate power management related controls when SATA is in AHCI mode. AHCI aware software will need to proceed to disabling all power management related controls outlined in AHCI spec.
	3. SATA_PCI_config 0x40 [0]= 0	Clears the bit to lock configuration registers so that AHCI HBA Capabilities Register is read-only.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
X								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

6.13 Optionally Turning On/Off SATA AHCI HBA Capabilities (For SB600 All Revisions)

This section outlines the details about adding the abilities for turning on/off SATA HBA Capabilities. In doing so, some AHCI HBA Capabilities can be optionally turned on/off.

Once one particular capability is decided to be turned on/off, the following programming sequence has to apply, for that capability. For example, if one wants to turn on/off CAP.SALP (Support for Aggressive Link Power Management), the programming sequence will be 1, 2a, and then 3, as described in the Register Settings.

Five SATA AHCI HBA Capabilities can be turned on/off, within the following four groups:

- (a) CAP.SALP: Support for Aggressive Link Power Management
- (b) CAP.SPM: Support for Port Multiplier
- (c) CAP.SSC and CAP.PSC: Support for Slumber State Capable and Support for Partial State Capable
- (d) PxCMD.HPCP: Hot Plug Capable Port

ASIC Rev	Register Settings	Function/Comment
1. SB600 All Revisions	1. SATA_PCI_config 0x40 [0] = 1	Unlocks the configuration register so that HBA AHCI Capabilities Register can be modified.
2. a. SB600 All revisions b. SB600 All Revisions c. SB600 A21 and above d. SB600 A21 and above 3. SB600 All Revisions	2. a. SATA_BAR5 + 0xFC [11] = 0(off) or 1(on) (Programming this in A13 and below will have no effect. For A13 and below, this register setting should NOT overwrite the values found in section *6.10*). b. SATA_BAR5 + 0xFC [12] = 0(off) or 1(on) (This is applicable to all SB600 revisions) c. SATA_BAR5 + 0xFC [27] = 0(on) or 1(off) (Programming this in A13 and below will have no effect. For A13 and below, this register setting should NOT overwrite the values found in section *6.12*). d. SATA_BAR5 + 0xFC[17] = 0(of) or 1(on) (Programming this bit will only take effect for A21 and above).	a. Setting this bit to 1/0 will turn on/off the Support-Aggressive-Link-Power-Management Capability in AHCI HBA Capabilities Register. Default is 1(on), for SB600 A21 and above. b. Setting this bit to 1/0 will turn on/off the Support-Port-Multiplier Capability in AHCI HBA Capabilities Register. Default is 1(on), for SB600 all revisions. c. Setting this bit to 1/0 will turn off/on both the Support-Partial-State and Support-Slumber-State Capabilities in AHCI HBA Capabilities Register. Please note the polarity of on and off: 1=off, 0=on. Default is 0 (on), for SB600 A21 and above. d. Setting this bit to 1/0 will indicate whether all 4 SATA ports are hot plug capable, and it sets PxCMD.HPCP accordingly. The default is 1 (on), for SB600 A21 and above.
	3. SATA_PCI_config 0x40 [0]= 0	Clears the bit to lock configuration registers so that AHCI HBA Capabilities Register is read-only.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	**For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx**
X								
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

7 LPC (bus-0, dev-20, fun-03)

7.1 Enabling/Disabling LPC Controller (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0x64 [20] = 1	Enables the LPC controller.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.2 Enabling LPC DMA Function (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	LPC_PCI_config 0x40 [2] = 1	Enables DMA transaction on the LPC bus. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
						X		
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.3 Disabling LPC TimeOut (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	LPC_PCI_config 0x48 [7] = 0	Disables the timeout mechanism on LPC. If the peripheral has a long latency cycle when driving the SYNC field of the LPC bus, the LPC will not drop the cycle. An example of a long latency cycle is accessing SMC SIO with parallel port address 0x37C.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
						X		
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.4 Parallel Port ECP Mode Support (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	If IO 0x378 & IO 0x778 as ECP (or ECP+EPP) address port is used: LPC_PCI_config 0x44 [0] = 1 LPC_PCI_config 0x44 [1] = 1 If IO 0x278 & IO 0x678 as ECP (or ECP+EPP) address port is used: LPC_PCI_config 0x44 [2] = 1 LPC_PCI_config 0x44 [3] = 1 If IO 0x3BC & IO 0x7BC as ECP (or ECP+EPP) address port is used: LPC_PCI_config 0x44 [4] = 1 LPC_PCI_config 0x44 [5] = 1	For the parallel port to support ECP mode, or ECP+EPP mode, the SBIOS needs to allocate 2 base addresses for the parallel port. base_address_2 = base_address_1 + 0x400 Base_address_1 is controlled by register bit 0, or bit 2, or bit 4. Base address_2 is controlled by register bit 1, or bit 3, or bit 5. The SBIOS needs to enable both base addresses to properly support ECP (or ECP+EPP) mode.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
						X		
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

7.5 Disabling LPC MSI Capability (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	LPC_PCI_config 0x78 [1] = 0	Disables MSI capability.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
						X		
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

8 AC97 Audio (bus-0, dev-20, fun-05)

8.1 Enabling/Disabling AC97 Audio (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x59 [0] = 1	Disables the AC97 audio controller. When this bit is set, the AC97 audio controller PCI configuration space will not be visible to software.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

8.2 Revision ID (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	AC97_Audio_PCI_config 0x08 = 00	Revision ID for AC97 audio controller.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
				X				
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

8.3 C3 Pop-Up (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	AC97_Audio_BAR0 0x80[1] = 1	If the CPU is K8, and C3PopUp function is enabled, then the BIOS should set this mirror bit to inform the ac97 driver that C3Pop-up is enabled. The driver will in turn not set the SetBusBusy bit in Memory_Mapped 0x04[14]

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
				X				
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

8.4 Disabling AC97 Audio MSI Capability (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	AC97_Audio_PCI_config 0x42[0] = 0	Disables MSI capability.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
				X				
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

9 AC97 Modem (bus-0, dev-20, fun-06)

9.1 Enabling/Disabling AC97 Modem (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x59 [1] = 1	Disables the AC97 modem controller. When this bit is set, the AC97 modem controller PCI configuration space will not be visible to software.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

9.2 Revision ID (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	AC97_Modem_PCI_config 0x08 = 00	Revision ID for AC97 Modem controller

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
				X				
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

9.3 Disabling AC97 Modem MSI Capability (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	AC97_Modem_PCI_config 0x42[0] = 0	Disables MSI capability.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
				X				
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

10 IDE Controller (bus-0, dev-20, fun-01)

The SB600 IDE controller supports single primary channel, even though resources of the secondary IDE channel are allocated by the in-box driver from the Microsoft operating system. Therefore the IDE programmable interface (IDE PCI config 0x09 bits [3:2]) is not recommended for modification.

10.1 Disabling IDE MSI Capability (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	IDE PCI_config 0x70 [16]=0	Disables MSI capability.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
			X					
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

10.2 Enabling IDE Data Bus DD7 Pull-down Resistor (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	ACPI PMIO2 0xE5 [2]=1	Enables IDE data bus DD7 pulling down resistor at IO pad all the time whenever IDE controller is enabled.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
			X					
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

11 HD Audio (bus-0, dev-20, fun-02)

11.1 Enabling/Disabling HD Audio (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	PM_IO 0x59[3] = 1	0 = Disables the HD Audio controller 1 = Enables the HD Audio controller

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

11.2 HD Audio Interrupt Routing Table (for All Revisions)

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_config 0x63[2:0] = 110 (default)	Interrupt routing table for HD Audio: 000 = INTA# 001 = INTB# 010 = INTC# 011 = INTD# 100 = INTE# 101 = INTF# 110 = INTG# 111 = INTH#

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx
		X						
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

11.3 Audio Port Configuration (for All Revisions)

This register controls the selection of ACZ_SDIN0/GPIO42, ACZ_SDIN1/GPIO43, ACZ_SDIN2/GPIO44, and AZ_SDIN3/GPIO46 pins to function as GPIO, AC97, or HD Audio signals.

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_Config_Extend_Reg 0x00[1:0] = 01 (default)	Port 0 configuration for HD Audio/AC97/GPIO: 00 or 11 = GPIO 01 = AC97 10 = HD Audio Note: Port 0 refers to the ACZ_SDIN0/GPIO42 pin.
All Revs SB600	SMbus_PCI_config_Extend_Reg 0x00[3:2] = 01 (default)	Port 1 configuration for HD Audio/AC97/GPIO: 00 or 11 = GPIO 01 = AC97 10 = HD Audio Note: Port 1 refers to the ACZ_SDIN1/GPIO43 pin.

ASIC Rev	Register Settings	Function/Comment
All Revs SB600	Smbus_PCI_Config_Extend_Reg 0x00[5:4] = 10 (default)	Port 2 configuration for HD Audio/AC97/GPIO: 00 or 11 = GPIO 01 = AC97 10 = HD Audio Note: Port 2 refers to the ACZ_SDIN2/GPIO44 pin.
All Revs SB600	Smbus_PCI_Config_Extend_Reg 0x00[7:6] = 10 (default)	Port 3 configuration for HD Audio/AC97/GPIO: 00 or 11 = GPIO 01 = AC97 10 = HD Audio Note: Port 3 is the AZ_SDIN3/GPIO46 pin.

Note: The Smbus_PCI_Config_Extend_Reg are indirectly accessed registers that are accessed through Smbus_PCI_config xF8 (ExtendedAddrPort) and Smbus_PCI_config xFC (ExtendedDataPort). Refer to the *AMD SB600 Register Reference Manual*, SMBUS section describing the PCI config xF8/FC details.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	**For register details refer to the sections check-marked in the register reference guide RRG-xxxSB600-xx**
		X						
RTC	**ACPI**	**PM REG**	**A-LINK**	**I/O REG**	**XIOAPIC**			

Appendix: Revision History

Date	Revisions	PDF	Description
Oct 1, 2008	3.02	46156_sb600_rpr_pub_3.02	• First public release.