



**Family 10h**  
**AMD Phenom™ II Processor**  
**Product Data Sheet**



Publication # **46878**  
Revision: **3.05**  
Issue Date: **April 2010**

---

© 2009, 2010 Advanced Micro Devices, Inc. All rights reserved.

The contents of this document are provided in connection with Advanced Micro Devices, Inc. (“AMD”) products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. The information contained herein may be of a preliminary or advance nature and is subject to change without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in AMD’s Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

AMD’s products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD’s product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.

---

#### **Trademarks**

AMD, the AMD Arrow logo, AMD Phenom and combinations thereof, AMD CoolCore, AMD PowerNow!, Cool’n’Quiet, and 3DNow! are trademarks of Advanced Micro Devices, Inc.

HyperTransport is a licensed trademark of the HyperTransport Technology Consortium.

MMX is a trademark of Intel Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

---

## Revision History

| Date          | Revision | Description   |
|---------------|----------|---|
| April 2010    | 3.05     | Third Public Release. <ul style="list-style-type: none"><li>• Added six-core option</li><li>• Added AMD Turbo CORE Technology</li></ul>   |
| February 2009 | 3.04     | Second Public Release. <ul style="list-style-type: none"><li>• Updated brand-specific image on front page</li><li>• Added AM3 package and Socket AM3 Socket Infrastructure<ul style="list-style-type: none"><li>• Added support for DDR3 SDRAM, up to 667 MHz</li><li>• Increased HyperTransport™ 3.0 max data rate to 4400 MT/s</li></ul></li><li>• Added triple-core option</li><li>• Updated L3 configuration</li><li>• Removed statement about miscellaneous IO signals</li></ul> |
| January 2009  | 3.02     | Initial Public Release.   |

# 1 Family 10h AMD Phenom™ II Processor Features

The following is a list of features and capabilities of the Family 10h AMD Phenom™ II processor.

- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, SSE3, SSE4a, ABM, MMX™, 3DNow!™ technology and legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on the chip
- **AMD64 Technology**
  - AMD64 technology instruction-set extensions
  - 64-bit integer registers, 48-bit addresses
  - Sixteen 64-bit integer registers
  - Sixteen 128-bit SSE/SSE2/SSE3/SSE4a registers
- **Multi-Core Architecture**
  - Triple-core, quad-core, or six-core options
  - AMD Balanced Smart Cache
    - Discrete L1 and L2 cache structures for each core
    - Shared L3 cache structure
- **Machine-Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays
- **Cache Structures**
  - **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
    - Two 64-bit operations per cycle, 3-cycle latency
  - **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
    - With advanced branch prediction
  - **512-Kbyte 16-Way Associative ECC-Protected L2 Cache**
    - Exclusive cache architecture storage in addition to L1 caches
  - **6128-Kbyte (6-Mbyte) Maximum, 64-way Maximum Associative ECC-Protected L3 Cache**
    - Shared cache architecture storage in addition to exclusive L1 and L2 caches
    - 2-cycle latency improvement for Phenom II processors
- **Floating-Point Unit**
  - AMD Wide Floating-Point Accelerator
    - 128-bit Floating-Point Unit (FPU)
- **Virtualization Features**
  - SVM disable and lock
  - Nested paging
  - Rapid Virtualization Indexing
  - Improved world-switch speed for Phenom II processors
- **Power Management**
  - Multiple low-power states
  - AMD Cool'n'Quiet™ 3.0
    - 45-nm process for decreased power consumption
    - Enhanced AMD PowerNow!™ Technology
    - AMD Smart Fetch Technology
  - AMD CoolCore™ Technology
    - Enhanced L3 clock-gating for Phenom II processors
  - Dual Dynamic Power Management

- System Management Mode (SMM)
- ACPI-compliant, including support for processor performance states
- **AMD Turbo CORE Technology**
- Supported power states: C0, C1, C1E, S0, S1, S3, S4, S5
- **Electrical Interfaces**
  - DDR2 SDRAM: SSTL\_1.8 per JEDEC specification
  - DDR3 SDRAM: Compliant to JEDEC DDR3 1.5-V SDRAM specification
  - Refer to the *AMD Family 10h Processor Electrical Data Sheet*, order# 40014, for electrical details of AMD Family 10h processors.
- **HyperTransport™ Technology to I/O Devices**
  - HyperTransport 1 and HyperTransport 3 technology supported
  - One (1) link, 16-bits in each direction, supporting up to 2000 MT/s (4.0 GB/s) in each direction in HyperTransport Generation 1.0 mode and 4400 MT/s (8.8 GB/s) in each direction in HyperTransport Generation 3.0 mode.
- **Integrated Memory Controller**
  - AMD Memory Optimizer Technology
  - Low-latency, high-bandwidth
  - Adaptive Prefetching Support
  - ECC checking with double-bit detect and single-bit correct
  - Supports up to four unbuffered DIMMs
  - Package AM2r2
    - 144-bit DDR2 SDRAM controller operating at frequencies up to 1066 MT/s (533 MHz)
  - Package AM3
    - 144-bit DDR3 SDRAM controller operating at frequencies up to 1333 MT/s (667 MHz)
- **Available Packages**
  - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
  - Package AM2r2
    - Refer to the *AM2r2 Processor Functional Data Sheet*, order# 41697, for functional and mechanical details of the AM2r2 package processor.
    - 940-pin lidded micro PGA
    - 1.27-mm pin pitch
    - 31 x 31 row pin array
    - Organic C4 die attach
  - Package AM3
    - Refer to the *AM3 Processor Functional Data Sheet*, order# 40778, for functional and mechanical details of the AM3 socket.
    - 938-pin lidded micro PGA
    - 1.27-mm pin pitch
    - 31 x 31 row pin array
    - Organic C4 die attach

## 2 Compatible Socket Infrastructures

Refer to the *AMD Infrastructure Roadmap*, order# 41842 for information on platform-feature implications of package and socket-infrastructure combinations. Family 10h AMD Phenom™ II processors support the following socket infrastructures:

- **Socket AM2r2 Socket Infrastructure**
  - Compatible with AM2, AM2r2, and AM3 package processors
  - Refer to the *AM2r2 Processor Functional Data Sheet*, order# 41697, for functional and mechanical details of the AM2r2 socket.
- **Socket AM3 Socket Infrastructure**
  - Compatible with AM3 package processors
  - Refer to the *AM3 Processor Functional Data Sheet*, order# 40778, for functional and mechanical details of the AM3 socket.