Family 10h
AMD Phenom™ II Processor
Product Data Sheet

Publication # **46878**
Revision: **3.05**
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Revision History

Date	Revision	Description
April 2010	3.05	Third Public Release. • Added six-core option • Added AMD Turbo CORE Technology

February 2009	3.04	Second Public Release.
		• Updated brand-specific image on front page
		• Added AM3 package and Socket AM3 Socket Infrastructure
		  • Added support for DDR3 SDRAM, up to 667 MHz
		  • Increased HyperTransport™ 3.0 max data rate to 4400 MT/s
		• Added triple-core option
		• Updated L3 configuration
		• Removed statement about miscellaneous IO signals

January 2009	3.02	Initial Public Release.

1 Family 10h AMD Phenom™ II Processor Features

The following is a list of features and capabilities of the Family 10h AMD Phenom™ II processor.

- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, SSE3, SSE4a, ABM, MMX™, 3DNow!™ technology and legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on the chip
- **AMD64 Technology**
  - AMD64 technology instruction-set extensions
  - 64-bit integer registers, 48-bit addresses
  - Sixteen 64-bit integer registers
  - Sixteen 128-bit SSE/SSE2/SSE3/SSE4a registers
- **Multi-Core Architecture**
  - Triple-core, quad-core, or six-core options
  - AMD Balanced Smart Cache
    - Discrete L1 and L2 cache structures for each core
    - Shared L3 cache structure
- **Machine-Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays
- **Cache Structures**
  - **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
    - Two 64-bit operations per cycle, 3-cycle latency
  - **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
    - With advanced branch prediction
  - **512-Kbyte 16-Way Associative ECC-Protected L2 Cache**
    - Exclusive cache architecture storage in addition to L1 caches
  - **6128-Kbyte (6-Mbyte) Maximum, 64-way Maximum Associative ECC-Protected L3 Cache**
    - Shared cache architecture storage in addition to exclusive L1 and L2 caches
    - 2-cycle latency improvement for Phenom II processors
- **Floating-Point Unit**
  - AMD Wide Floating-Point Accelerator
    - 128-bit Floating-Point Unit (FPU)
- **Virtualization Features**
  - SVM disable and lock
  - Nested paging
  - Rapid Virtualization Indexing
  - Improved world-switch speed for Phenom II processors
- **Power Management**
  - Multiple low-power states
  - AMD Cool‘n’Quiet™ 3.0
    - 45-nm process for decreased power consumption
    - Enhanced AMD PowerNow!™ Technology
    - AMD Smart Fetch Technology
  - AMD CoolCore™ Technology
    - Enhanced L3 clock-gating for Phenom II processors
  - Dual Dynamic Power Management

- System Management Mode (SMM)
- ACPI-compliant, including support for processor performance states
- AMD Turbo CORE Technology
- Supported power states: C0, C1, C1E, S0, S1, S3, S4, S5

- **Electrical Interfaces**
  - DDR2 SDRAM: SSTL_1.8 per JEDEC specification
  - DDR3 SDRAM: Compliant to JEDEC DDR3 1.5-V SDRAM specification
  - Refer to the *AMD Family 10h Processor Electrical Data Sheet*, order# 40014, for electrical details of AMD Family 10h processors.
- **HyperTransport™ Technology to I/O Devices**
  - HyperTransport 1 and HyperTransport 3 technology supported
  - One (1) link, 16-bits in each direction, supporting up to 2000 MT/s (4.0 GB/s) in each direction in HyperTransport Generation 1.0 mode and 4400 MT/s (8.8 GB/s) in each direction in HyperTransport Generation 3.0 mode.
- **Integrated Memory Controller**
  - AMD Memory Optimizer Technology
  - Low-latency, high-bandwidth
  - Adaptive Prefetching Support
  - ECC checking with double-bit detect and single-bit correct
  - Supports up to four unbuffered DIMMs
  - Package AM2r2
    - 144-bit DDR2 SDRAM controller operating at frequencies up to 1066 MT/s (533 MHz)
  - Package AM3
    - 144-bit DDR3 SDRAM controller operating at frequencies up to 1333 MT/s (667 MHz)
- **Available Packages**
  - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
  - Package AM2r2
    - Refer to the *AM2r2 Processor Functional Data Sheet*, order# 41697, for functional and mechanical details of the AM2r2 package processor.
    - 940-pin lidded micro PGA
    - 1.27-mm pin pitch
    - 31 x 31 row pin array
    - Organic C4 die attach
  - Package AM3
    - Refer to the *AM3 Processor Functional Data Sheet*, order# 40778, for functional and mechanical details of the AM3 socket.
    - 938-pin lidded micro PGA
    - 1.27-mm pin pitch
    - 31 x 31 row pin array
    - Organic C4 die attach

2 Compatible Socket Infrastructures

Refer to the *AMD Infrastructure Roadmap*, order# 41842 for information on platform-feature implications of package and socket-infrastructure combinations. Family 10h AMD Phenom™ II processors support the following socket infrastructures:

- **Socket AM2r2 Socket Infrastructure**
  - Compatible with AM2, AM2r2, and AM3 package processors
  - Refer to the *AM2r2 Processor Functional Data Sheet*, order# 41697, for functional and mechanical details of the AM2r2 socket**.**
- **Socket AM3 Socket Infrastructure**
  - Compatible with AM3 package processors
  - Refer to the *AM3 Processor Functional Data Sheet*, order# 40778, for functional and mechanical details of the AM3 socket.