Revision History

<table>
<thead>
<tr>
<th>Date</th>
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<tr>
<td>February 2011</td>
<td>3.05</td>
<td>Initial Public Release.</td>
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1 Family 10h AMD Athlon™ II Processor Features

The following is a list of features and capabilities of the Family 10h AMD Athlon™ II processor.

- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, SSE3, SSE4a, ABM, MMX™, 3DNow!™ technology and legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on the chip

- **AMD64 Technology**
  - AMD64 technology instruction-set extensions
  - 64-bit integer registers, 48-bit addresses
  - Sixteen 64-bit integer registers
  - Sixteen 128-bit SSE/SSE2/SSE3 registers

- **Multi-Core Architecture**
  - Dual-core, triple-core, or quad-core options
  - AMD Balanced Smart Cache
    - Discrete L1 and L2 cache structures for each core

- **Machine-Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays

- **Cache Structures**
  - **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
    - Two 64-bit operations per cycle, 3-cycle latency
  - **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
    - With advanced branch prediction
  - **512-Kbyte 16-Way Associative ECC-Protected L2 Cache**
    - Exclusive cache architecture storage in addition to L1 caches

- **Floating-Point Unit**
  - AMD Wide Floating-Point Accelerator
  - 128-bit Floating-Point Unit (FPU)

- **Management and Virtualization Features**
  - AMD Virtualization™ technology (AMD-V™)
    - Secure Virtualization Machine (SVM) disable and lock
    - Nested paging

- **Power Management**
  - Multiple low-power states
  - AMD CoolCore™ Technology
  - Dual Dynamic Power Management
  - System Management Mode (SMM)
  - ACPI-compliant, including support for processor performance states
  - Supported power states: C0, C1, C1E, S0, S1, S3, S4, S5

- **Electrical Interfaces**
  - DDR2 SDRAM: SSTL_1.8 per JEDEC specification
  - DDR3 SDRAM: Compliant with JEDEC DDR3 1.5-V SDRAM specification
  - Refer to the *AMD Family 10h Processor Electrical Data Sheet*, order# 40014, for electrical details of AMD Family 10h processors.

- **HyperTransport™ Technology to I/O Devices**
  - HyperTransport™ 1 and HyperTransport 3 technology supported
• One (1) link, 16-bits in each direction, supporting up to 2000 MT/s (4.0 GB/s) in each direction in HyperTransport Generation 1.0 mode and up to 4400 MT/s (8.8 GB/s) in each direction in HyperTransport Generation 3.0 mode

• Integrated Memory Controller
  • AMD Memory Optimizer technology
  • Low-latency, high-bandwidth
  • Adaptive prefetching support
  • ECC checking with double-bit detect and single-bit correct
  • Supports up to four unbuffered DIMMs
  • AM2r2 Socket Infrastructure
    • 144-bit DDR2 SDRAM controller operating at frequencies up to 1066 MT/s (533 MHz)
  • AM3 Socket Infrastructure
    • 144-bit DDR3 SDRAM controller operating at frequencies up to 1333 MT/s (667 MHz)

• Available Packages
  • Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
  • Package AM3
    • Refer to the *Socket AM3 Processor Functional Data Sheet*, order# 40778, for functional and mechanical details of the AM3 socket infrastructure.
    • 938-pin lidded micro PGA
    • 1.27-mm pin pitch
    • 31 x 31 row pin array
    • Organic C4 die attach
2 Compatible Socket Infrastructures

Refer to the *AMD Infrastructure Roadmap*, order# 41842 for information on platform-feature implications of package and socket infrastructure combinations. Family 10h AMD Athlon™ II processors support the following socket infrastructures:

- **AM2r2 Socket Infrastructure**
  - Compatible with AM2, AM2r2, and AM3 package processors
  - Refer to the *AM2r2 Processor Functional Data Sheet*, order# 41697, for functional and mechanical details of the AM2r2 socket infrastructure.

- **AM3 Socket Infrastructure**
  - Compatible with AM3 package processors
  - Refer to the *Socket AM3 Processor Functional Data Sheet*, order# 40778, for functional and mechanical details of the AM3 socket infrastructure.